

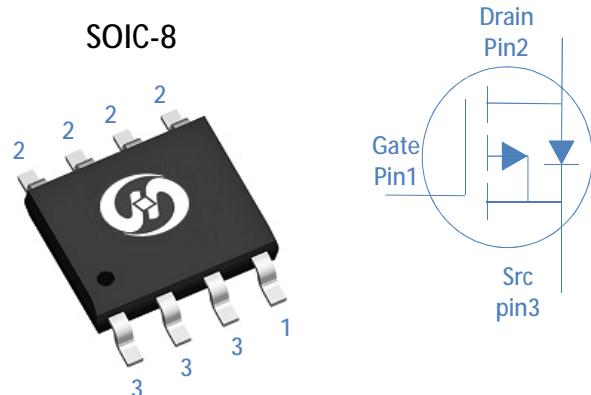
30V P-Ch Power MOSFET
Feature

- ◊ High Speed Power Switching, Logic Level
- ◊ Enhanced Avalanche Ruggedness
- ◊ 100% UIS Tested, 100% Rg Tested
- ◊ Lead Free, Halogen Free

V_{DS}	-30	V
$R_{DS(on),typ}$ $V_{GS}=10V$	14	$m\Omega$
$R_{DS(on),typ}$ $V_{GS}=4.5V$	21	$m\Omega$
I_D (Silicon Limited)	-9.3	A

Application

- ◊ Hard Switching and High Speed Circuit
- ◊ DC/DC in Telecoms and Industrial



Part Number	Package	Marking
HTS180P03T	SOIC-8	TS180P03T

Absolute Maximum Ratings at $T_j=25^\circ C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25^\circ C$	-9.3	A
Drain to Source Voltage	V_{DS}	-	-30	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	-37.2	A
Power Dissipation	P_D	$T_A=25^\circ C$	2.5	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	°C

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	°C/W

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_{\text{D}}=-250\mu\text{A}$	-0.8	-	-2.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-30\text{V}, T_j=25^\circ\text{C}$	-	-	-1	μA
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-4\text{A}$	-	14	18	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-2\text{A}$	-	21	26	

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-15\text{V}, f=1\text{MHz}$	-	1710	-	pF
Output Capacitance	C_{oss}		-	260	-	
Reverse Transfer Capacitance	C_{rss}		-	185	-	
Total Gate Charge	Q_g	$V_{\text{DD}}=-24\text{V}, I_{\text{D}}=-1\text{A}, V_{\text{GS}}=-4.5\text{V}$	-	18	-	nC
Gate to Source Charge	Q_{gs}		-	3.4	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	7.1	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$		-	16	-	
Rise time	t_r	$V_{\text{DD}}=-24\text{V}, I_{\text{D}}=-1\text{A}, V_{\text{GS}}=-10\text{V}, R_G=6\Omega$	-	8	-	ns
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	75	-	
Fall Time	t_f		-	36	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{F}}=-2\text{A}$	-		-1.2	V
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Fig 1. Typical Output Characteristics

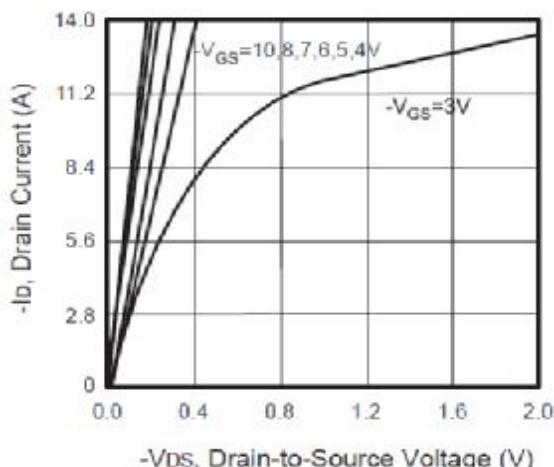


Figure 2. Gate Threshold Voltage vs. Junction Temperature

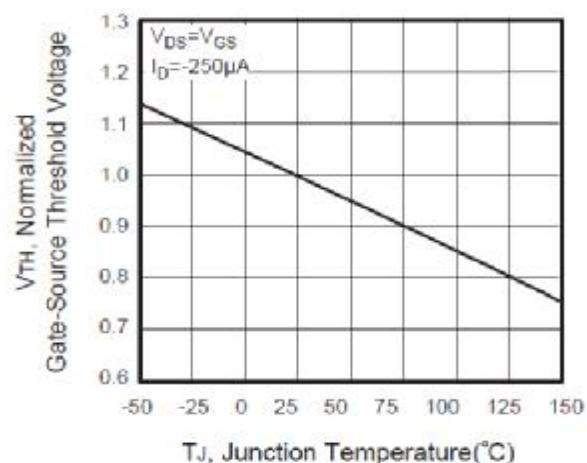


Figure 3. Breakdown Voltage vs. Junction Temperature

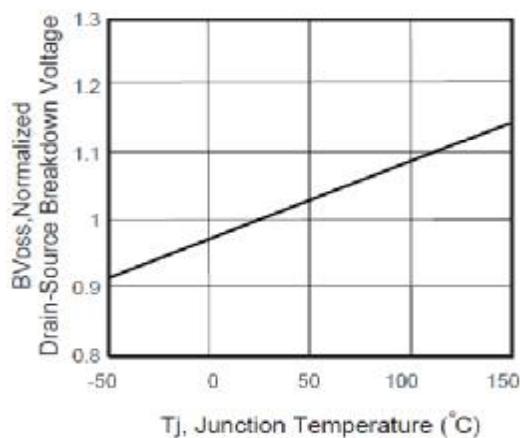


Figure 4. Normalized On-Resistance vs. Junction Temperature

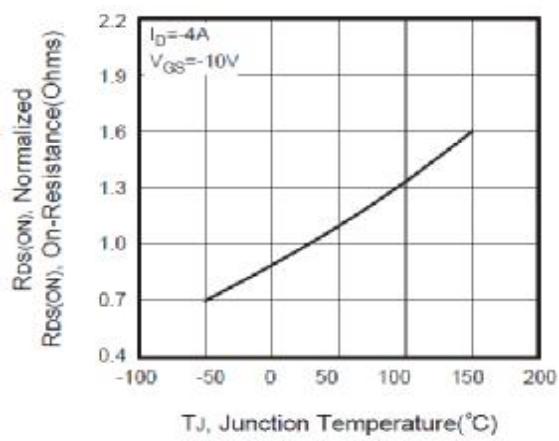


Figure 5. Typical Transfer Characteristics

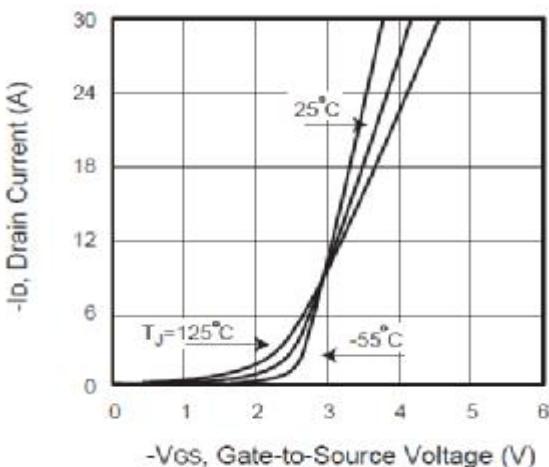


Figure 6. Typical Source-Drain Diode Forward Voltage

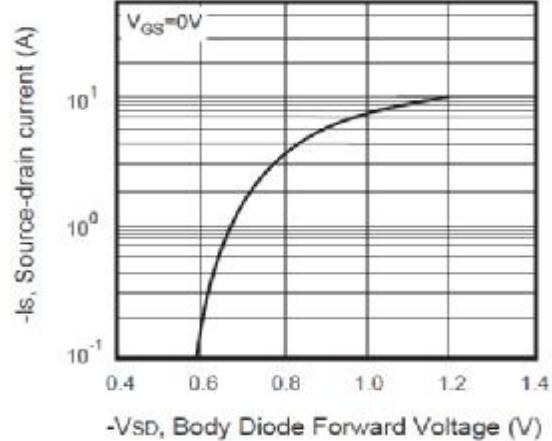


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

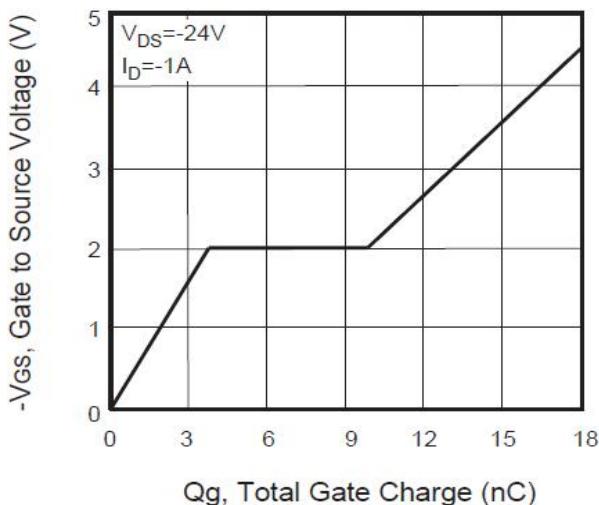


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

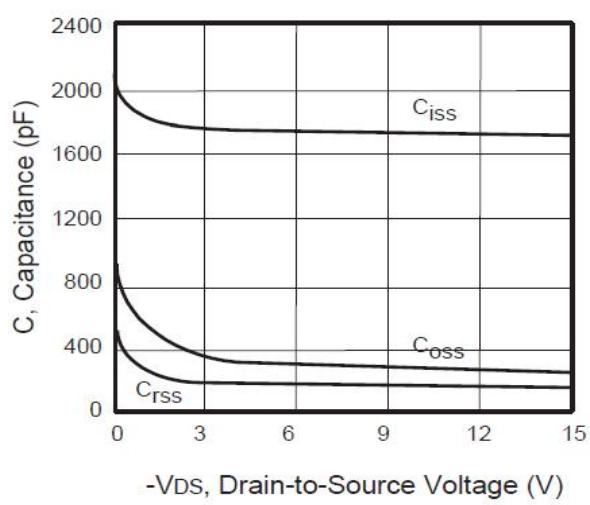


Figure 9. Maximum Safe Operating Area

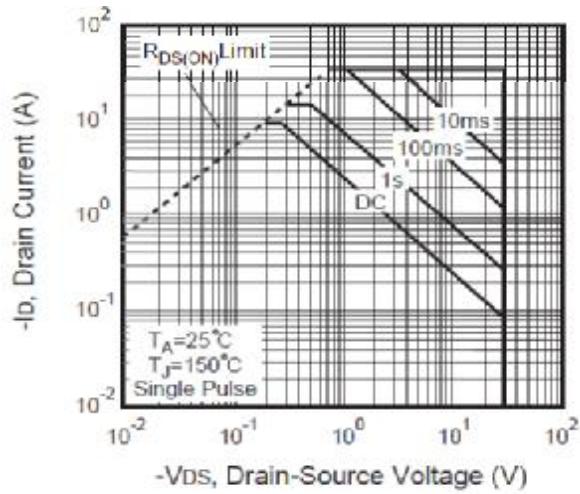
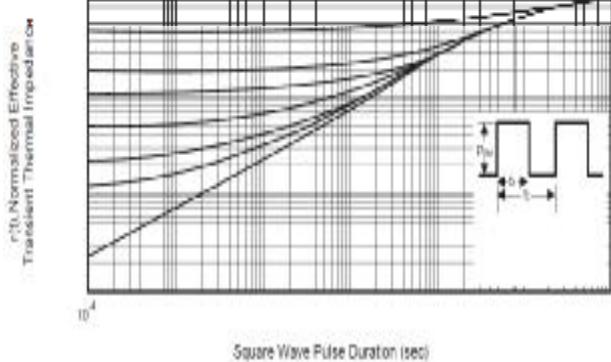
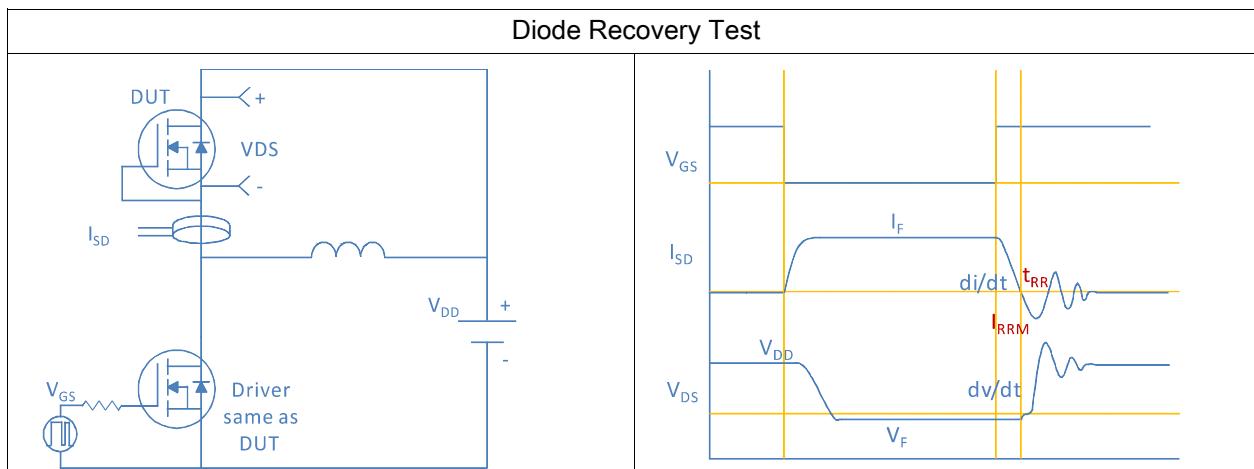
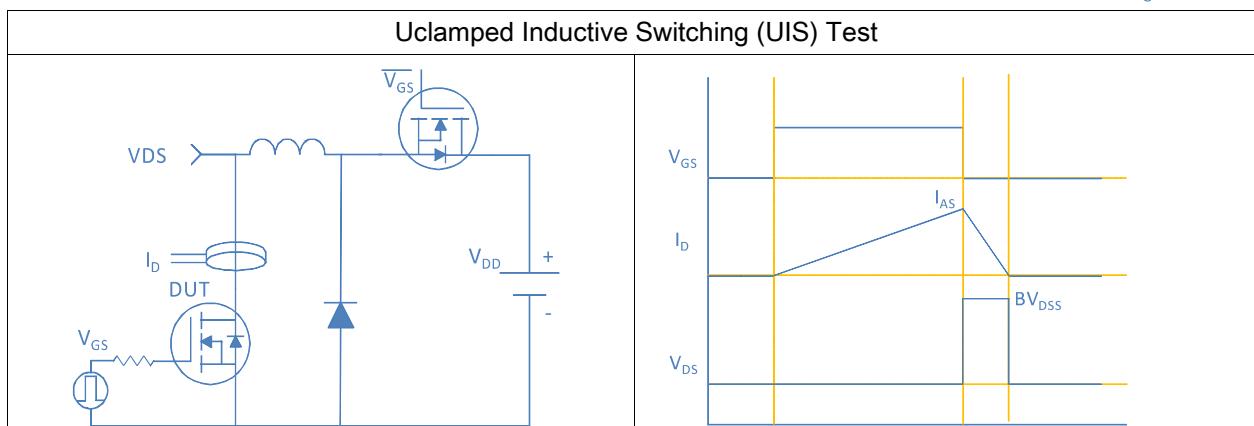
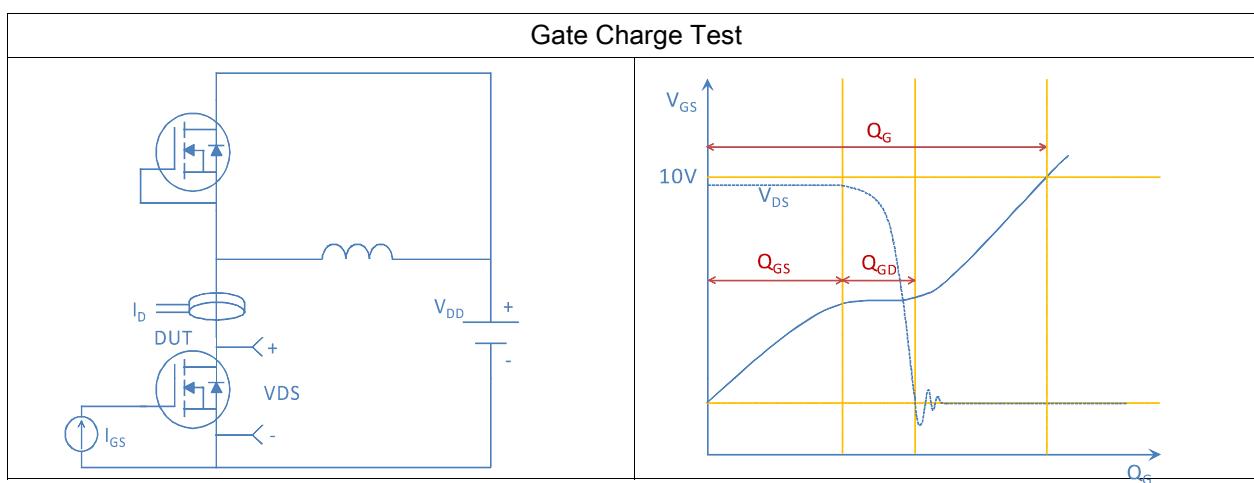
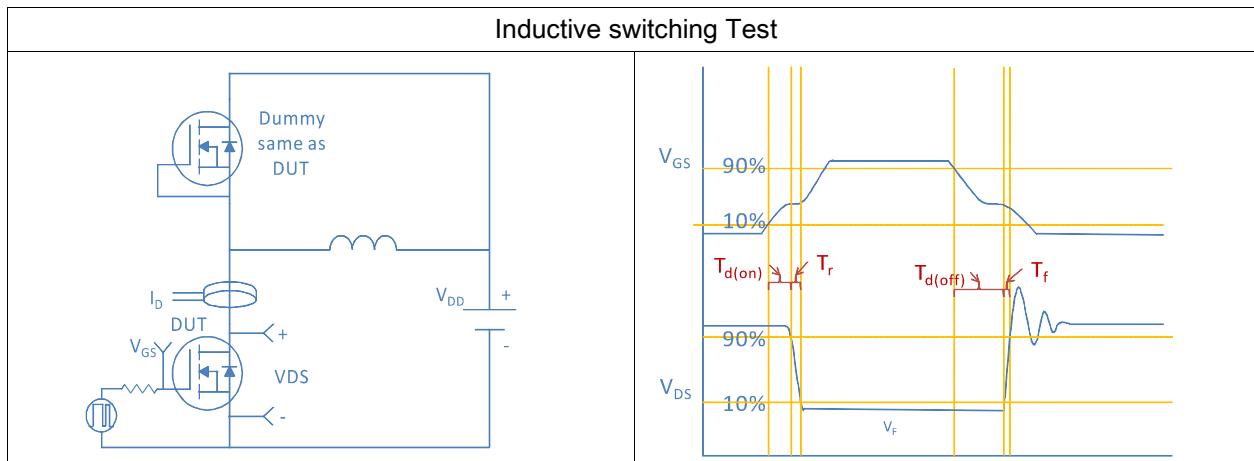
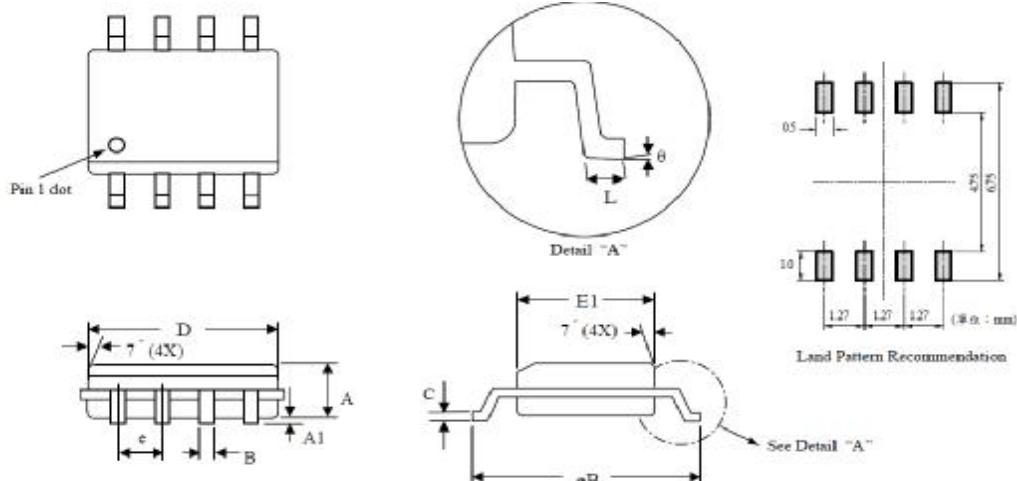


Figure 10. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





Package Outline
SOIC-8, 8 Leads


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.049	0.069
A1	0.10	0.25	0.004	0.010
B	0.31	0.51	0.012	0.020
C	0.17	0.25	0.007	0.010
D	4.69	5.00	0.185	0.197
E1	3.70	4.06	0.146	0.160
eB	5.80	6.20	0.228	0.244
e	1.27		0.050	
L	0.40	0.95	0.016	0.037
θ	0°		8°	