

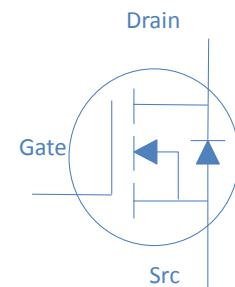
100V N-Ch Power MOSFET
Feature

- ◇ Optimized for high speed smooth switching, Logic level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested

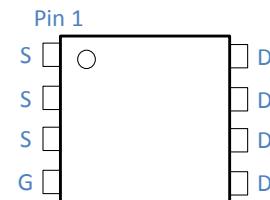
V_{DS}	100	V
$R_{DS(on),typ}$	$V_{GS}=10V$	4.6 mΩ
$R_{DS(on),typ}$	$V_{GS}=4.5V$	5.6 mΩ
I_D (Silicon Limited)	115	A
I_D (Package Limited)	60	A

Application

- ◇ DC-DC Conversion
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ SSR

DFN5x6


Part Number	Package	Marking
HGN052N10SL	DFN5x6	GN052N10SL


Absolute Maximum Ratings at $T_j=25^\circ C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25^\circ C$	115	A
Continuous Drain Current (Package Limited)		$T_C=100^\circ C$	73	
Continuous Drain Current (Package Limited)		$T_C=25^\circ C$	60	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	300	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.3mH, T_C=25^\circ C$	240	mJ
Power Dissipation	P_D	$T_C=25^\circ C$	125	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	°C

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	R_{eJC}	1	°C/W
Thermal Resistance Junction-Ambient	R_{eJA}	50	°C/W

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$	100	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_D=250\mu\text{A}$	1.4	1.7	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=100\text{V}, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=100\text{V}, T_j=100^\circ\text{C}$	-	-	100	
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=10\text{V}, I_D=20\text{A}$	-	4.6	5.2	m Ω
		$V_{\text{GS}}=4.5\text{V}, I_D=20\text{A}$	-	5.6	7	m Ω
Transconductance	g_{fs}	$V_{\text{DS}}=5\text{V}, I_D=20\text{A}$	-	70	-	S
Gate Resistance	R_G	$V_{\text{GS}}=0\text{V}, V_{\text{DS}} \text{ Open}, f=1\text{MHz}$	-	3.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=50\text{V}, f=1\text{MHz}$	-	4351	-	pF
Output Capacitance	C_{oss}		-	323	-	
Reverse Transfer Capacitance	C_{rss}		-	12	-	
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{DD}}=50\text{V}, I_D=20\text{A}, V_{\text{GS}}=10\text{V}$	-	60	-	nC
Total Gate Charge	$Q_g(4.5\text{V})$		-	26	-	
Gate to Source Charge	Q_{gs}		-	8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	10	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=50\text{V}, I_D=20\text{A}, V_{\text{GS}}=10\text{V}, R_G=10\Omega,$	-	15	-	ns
Rise time	t_r		-	6	-	
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	42	-	
Fall Time	t_f		-	8	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_F=20\text{A}$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=50\text{V}, I_F=20\text{A}, dI_F/dt=500\text{A}/\mu\text{s}$	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	275	-	nC

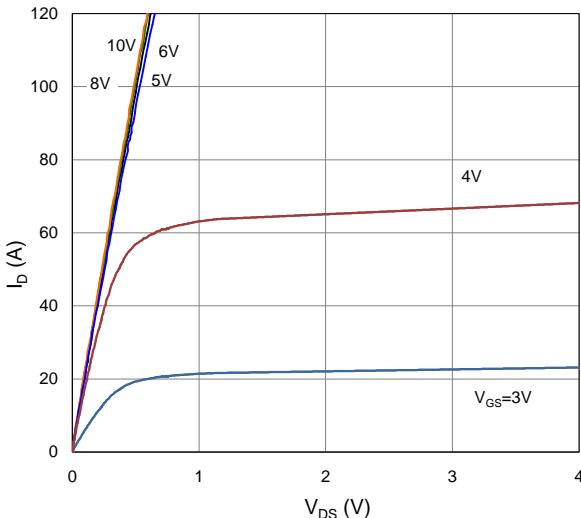
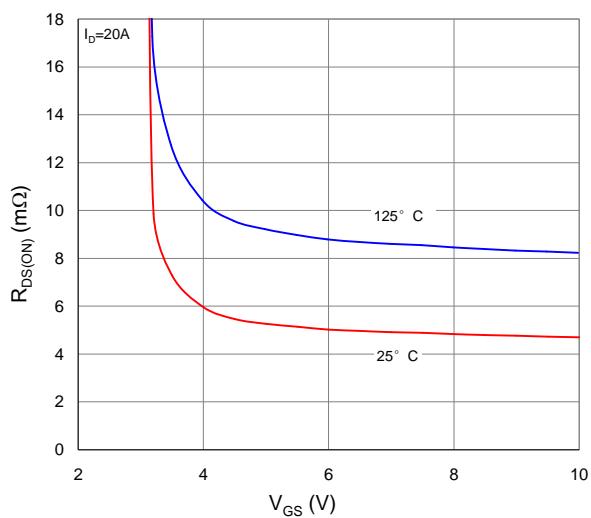
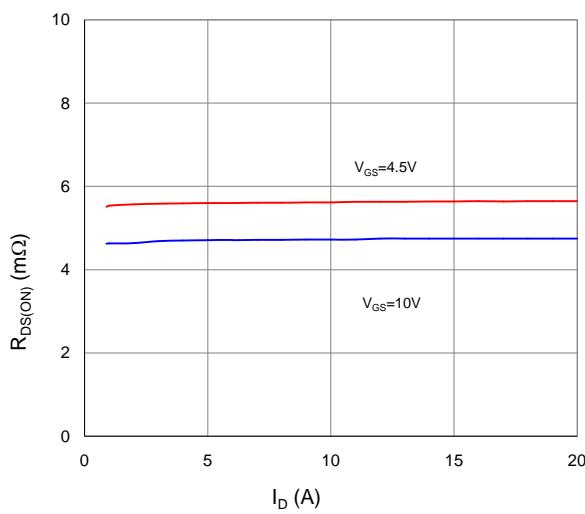
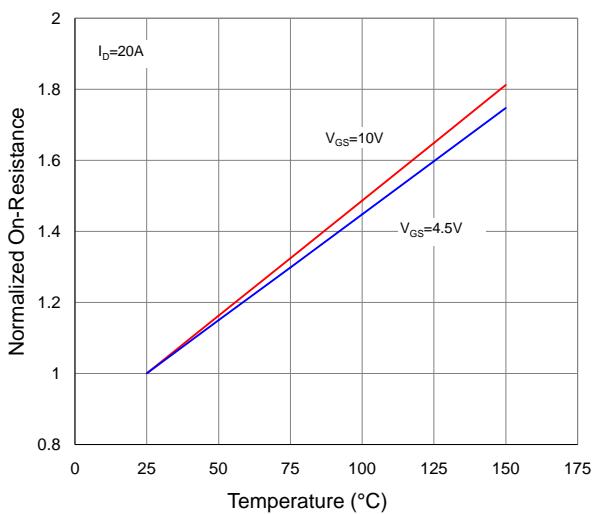
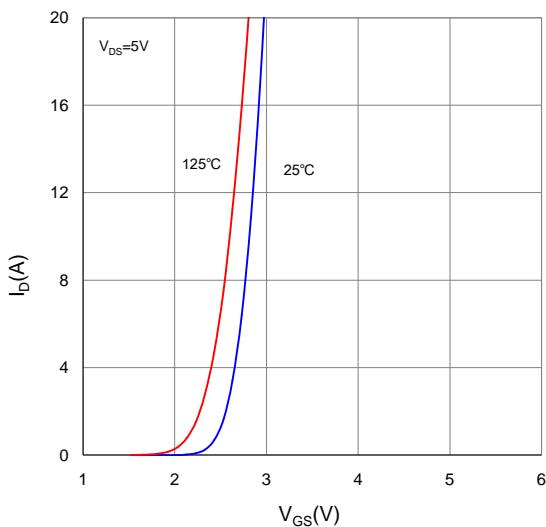
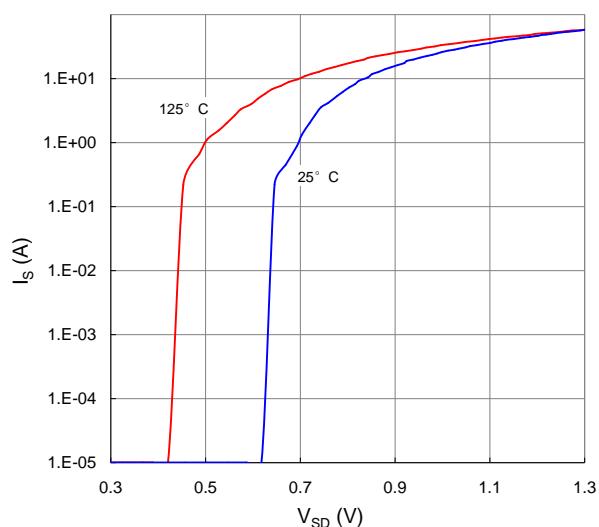
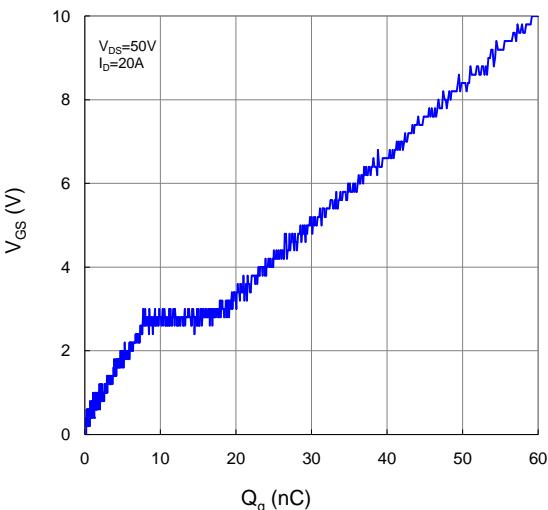
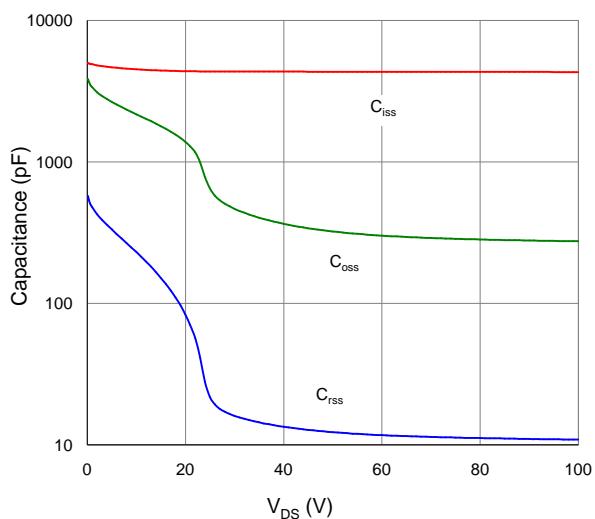
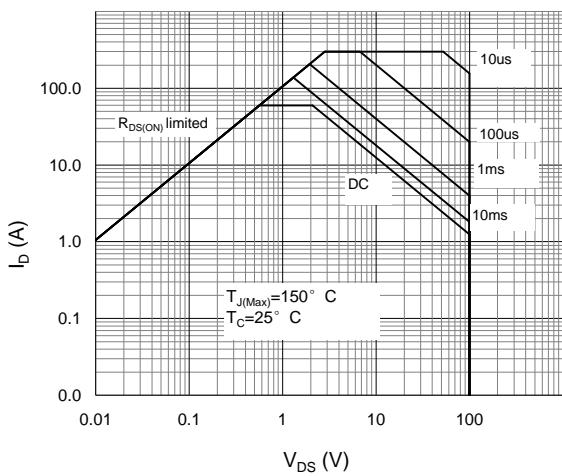
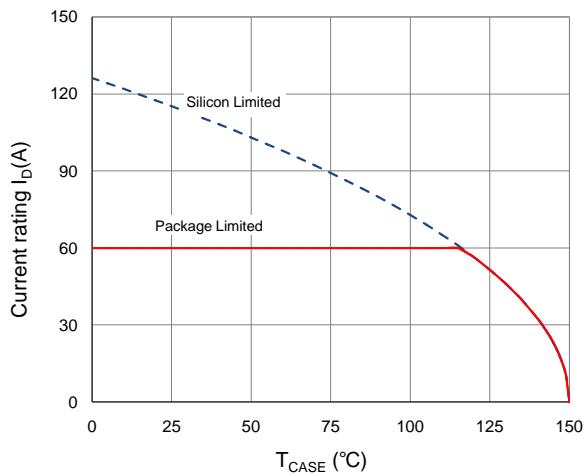
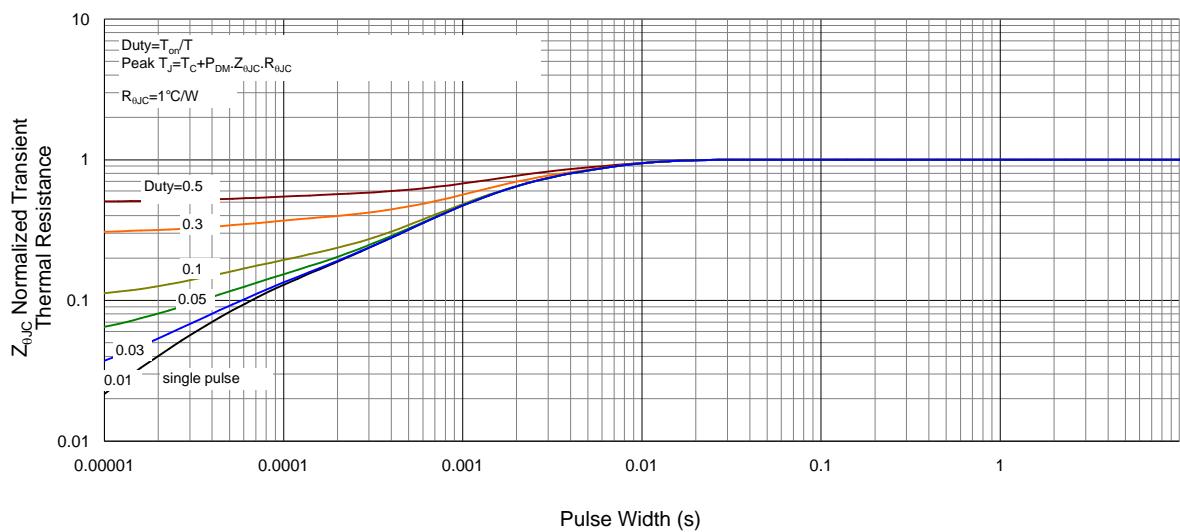
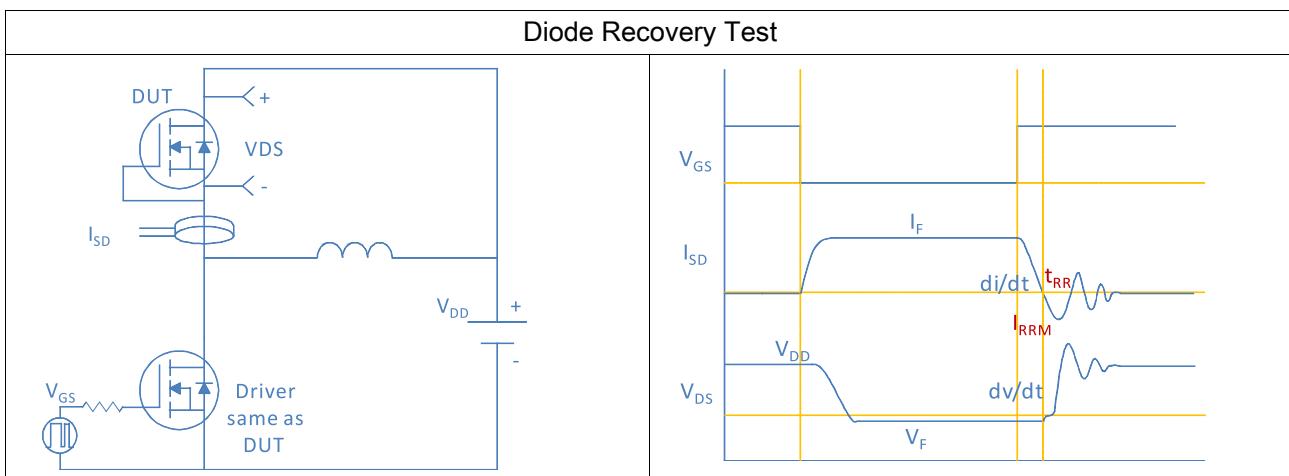
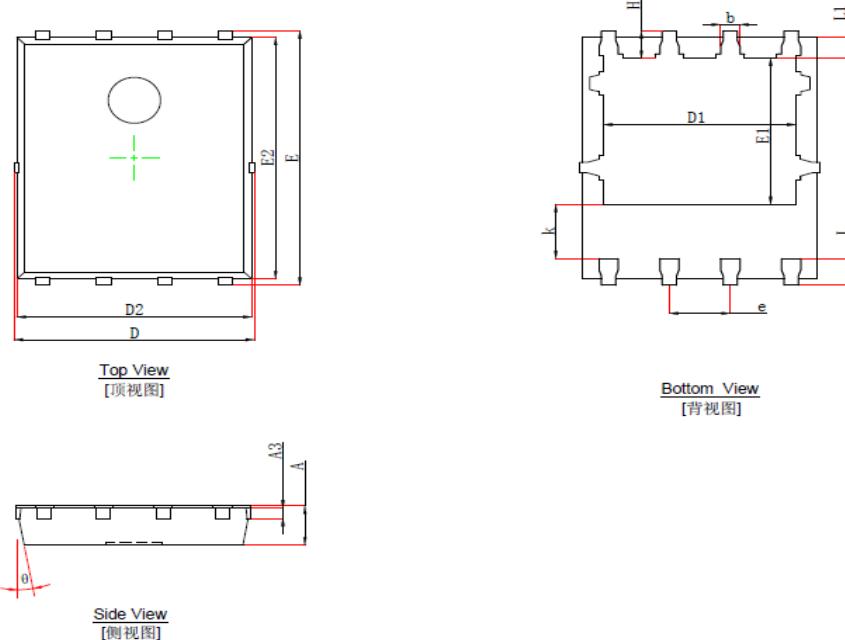
Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Transfer Characteristics

Figure 6. Typical Source-Drain Diode Forward Voltage


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case




Package Outline
DFN5x6_P, 8 Leads


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254 REF		0.010REF	
D	4.680	5.120	0.184	0.202
E	5.900	6.126	0.232	0.241
D1	3.610	4.110	0.142	0.162
E1	3.380	3.780	0.133	0.149
D2	4.800	5.000	0.189	0.197
E2	5.674	5.826	0.223	0.229
k	1.100	1.390	0.043	0.055
b	0.330	0.510	0.013	0.020
e	1.270TYP		1.270TYP	
L	0.510	0.711	0.020	0.028
L1	0.424	0.576	0.017	0.023
H	0.410	0.726	0.016	0.029
θ	0°	12°	0°	12°