

## 80V N-Ch Power MOSFET

### Feature

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free

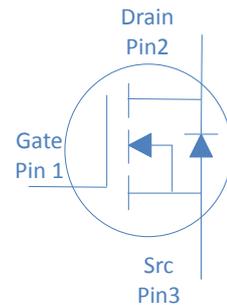
$V_{DS}$		80	V
$R_{DS(on),typ}$	$V_{GS}=10V$	4.3	mΩ
$R_{DS(on),typ}$	$V_{GS}=4.5V$	5.9	mΩ
$I_D$ (Silicon Limited)		63	A

### Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control

Part Number	Package	Marking
HGA058N08SL	TO-220F	GA058N08SL

TO-220F



### Absolute Maximum Ratings at $T_j=25^{\circ}C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^{\circ}C$	63	A
		$T_C=100^{\circ}C$	45	
Drain to Source Voltage	$V_{DS}$	-	80	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	380	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.3mH, T_C=25^{\circ}C$	240	mJ
Power Dissipation	$P_D$	$T_C=25^{\circ}C$	41.7	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 175	$^{\circ}C$

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	3.6	$^{\circ}C/W$
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	65	$^{\circ}C/W$

## Electrical Characteristics at T<sub>J</sub>=25°C (unless otherwise specified)

### Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	80	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	1	1.7	2.4	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =80V, T <sub>J</sub> =25°C	-	-	1	μA
		V <sub>GS</sub> =0V, V <sub>DS</sub> =80V, T <sub>J</sub> =100°C	-	-	100	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Drain to Source on Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A TO-220F	-	4.3	5.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A TO-220F	-	5.9	8.0	mΩ
Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	65	-	S
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> Open, f=1MHz	-	1.5	-	Ω

### Dynamic Characteristics

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =40V, f=1MHz	-	3130	-	pF
Output Capacitance	C <sub>oss</sub>		-	385	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	18	-	
Total Gate Charge (10V)	Q <sub>g</sub> (10V)	V <sub>DD</sub> =40V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	46	-	nC
Total Gate Charge (4.5V)	Q <sub>g</sub> (4.5V)		-	22	-	
Gate to Source Charge	Q <sub>gs</sub>		-	9	-	
Gate to Drain (Miller) Charge	Q <sub>gd</sub>		-	8	-	
Turn on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =40V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>G</sub> =10Ω,	-	11	-	ns
Rise time	t <sub>r</sub>		-	7	-	
Turn off Delay Time	t <sub>d(off)</sub>		-	38	-	
Fall Time	t <sub>f</sub>		-	9	-	

### Reverse Diode Characteristics

Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>F</sub> =20A	-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>R</sub> =40V, I <sub>F</sub> =20A, dI <sub>F</sub> /dt=400A/μs	-	48	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>		-	190	-	nC

Fig 1. Typical Output Characteristics

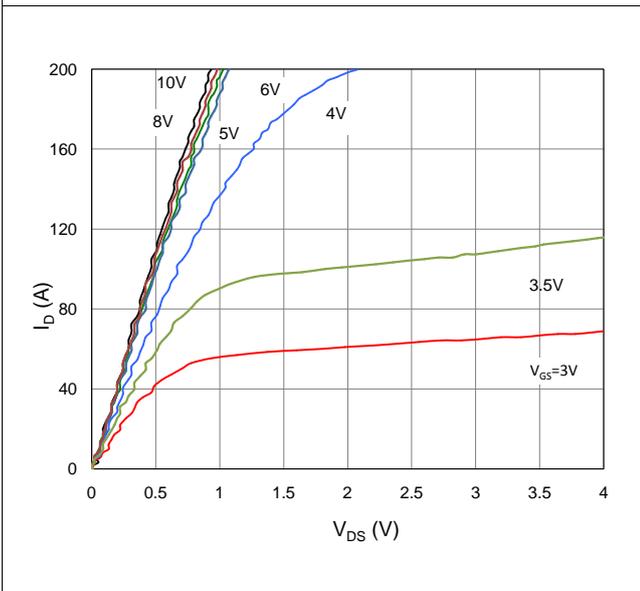


Figure 2. On-Resistance vs. Gate-Source Voltage

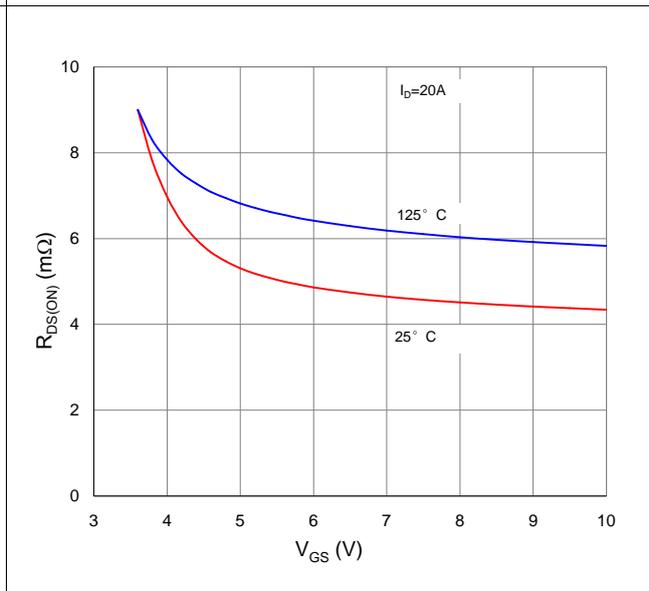


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

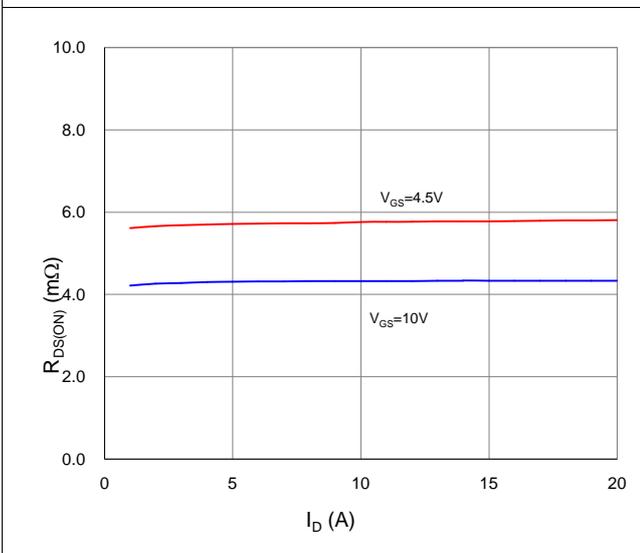


Figure 4. Normalized On-Resistance vs. Junction Temperature

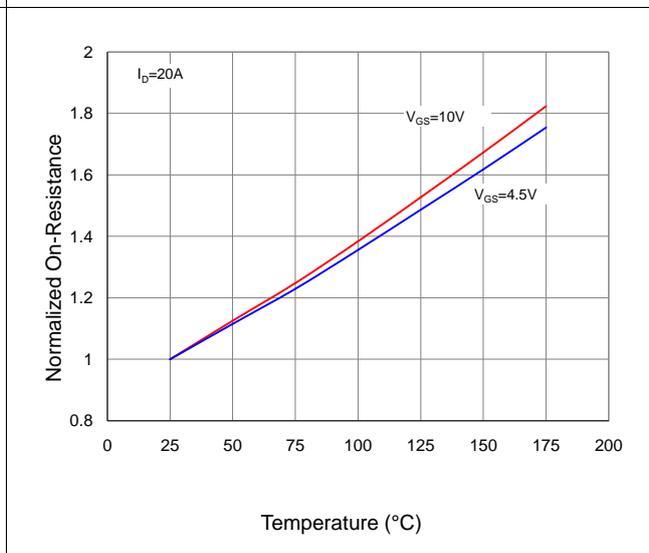


Figure 5. Typical Transfer Characteristics

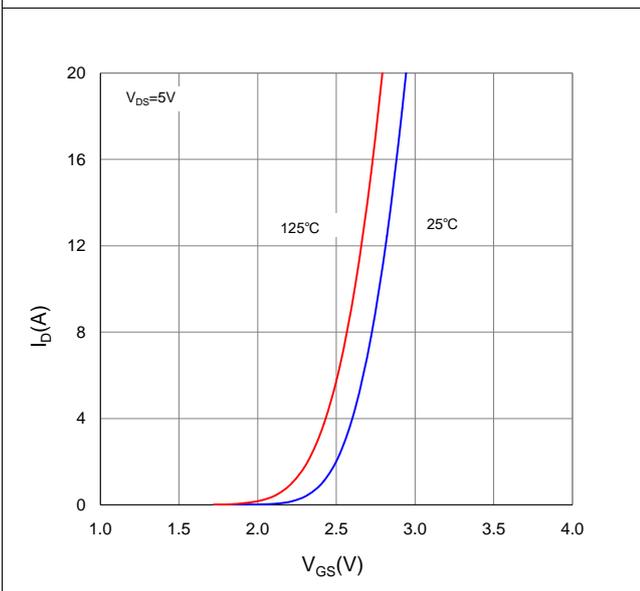


Figure 6. Typical Source-Drain Diode Forward Voltage

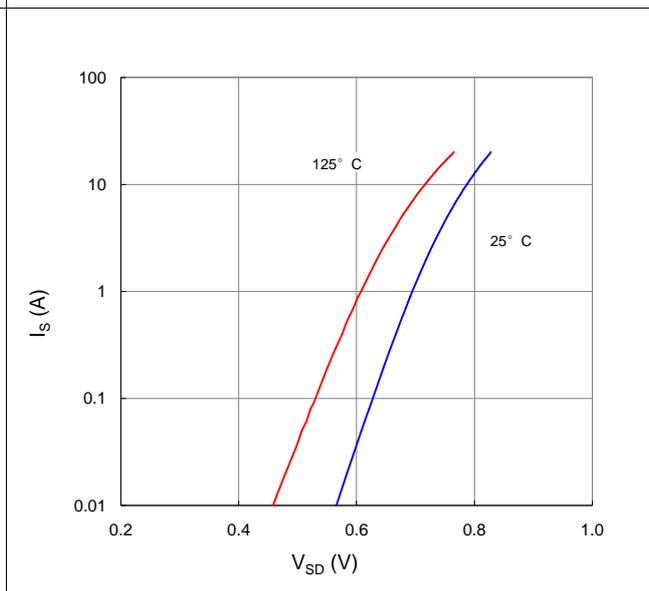


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

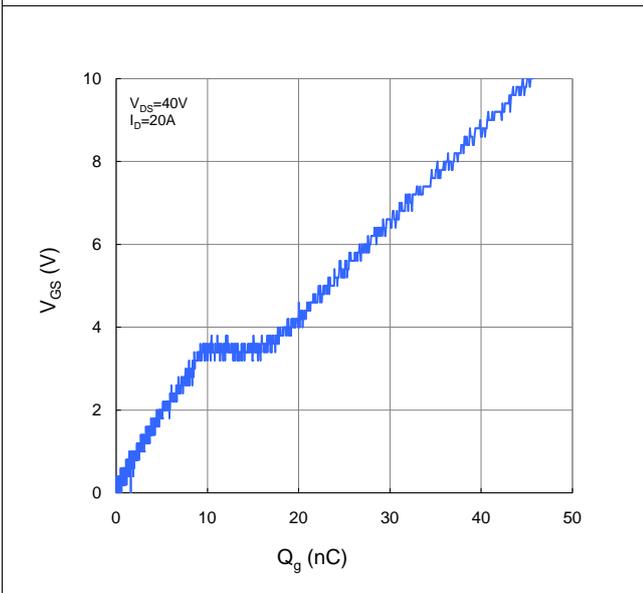


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

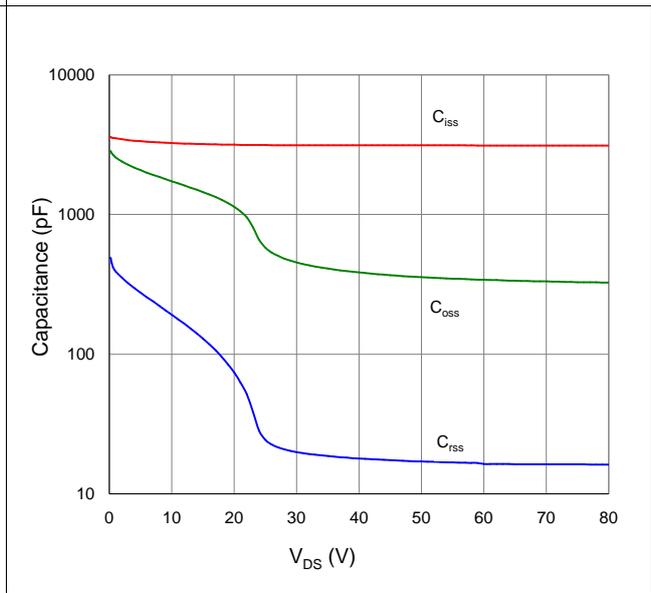


Figure 9. Maximum Safe Operating Area

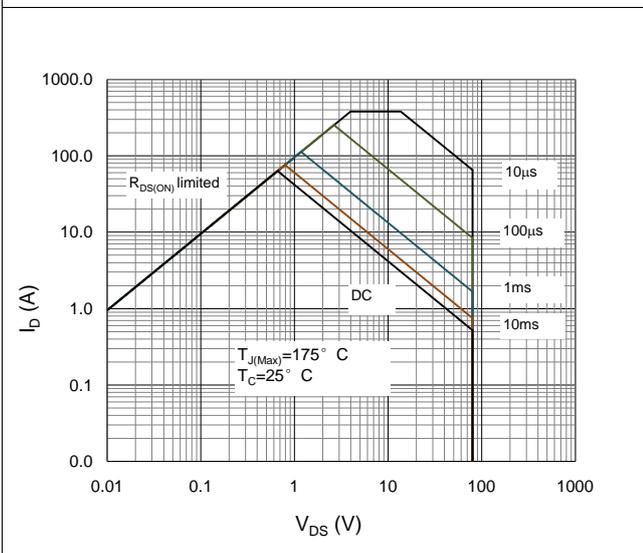


Figure 10. Maximum Drain Current vs. Case Temperature

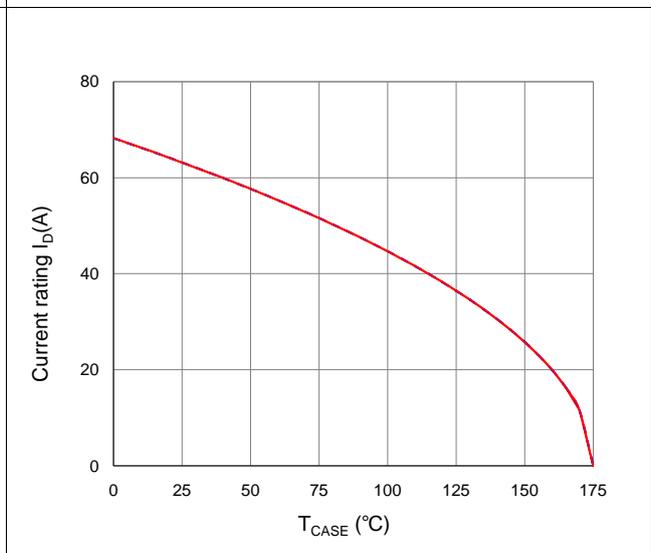
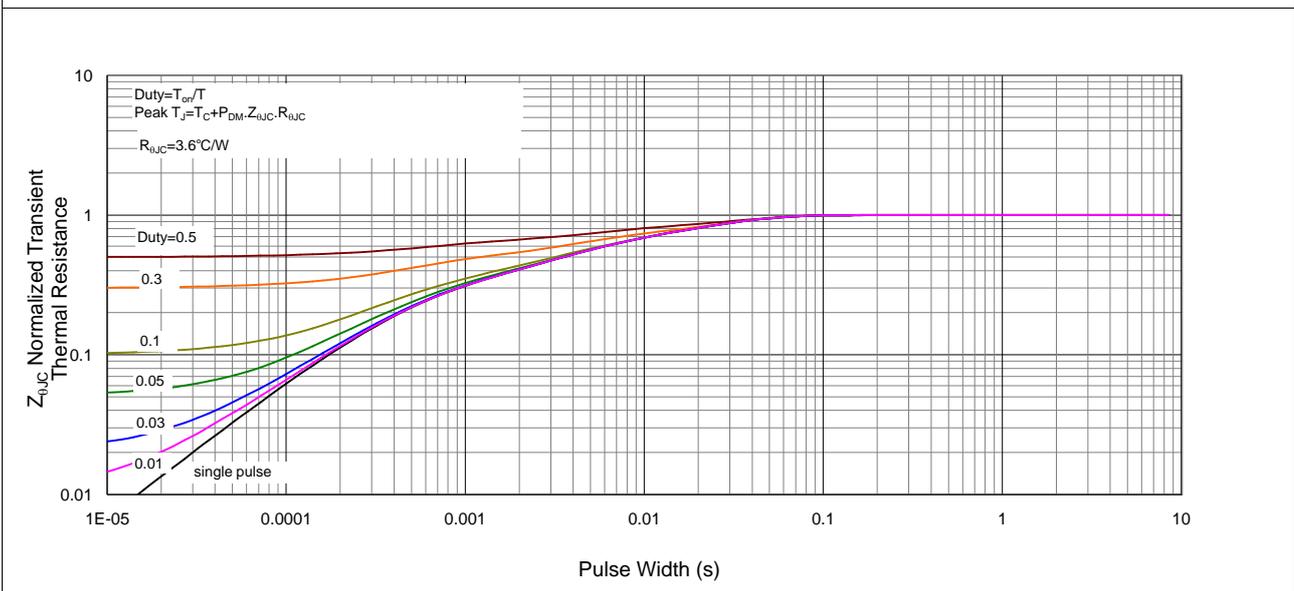
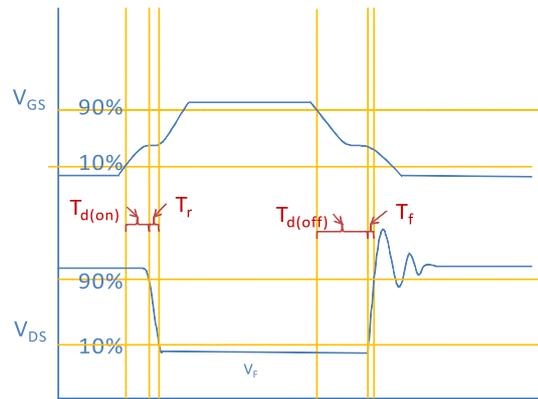
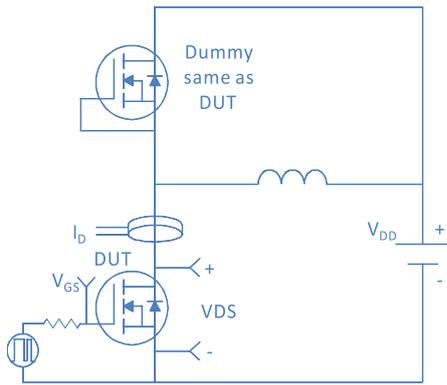


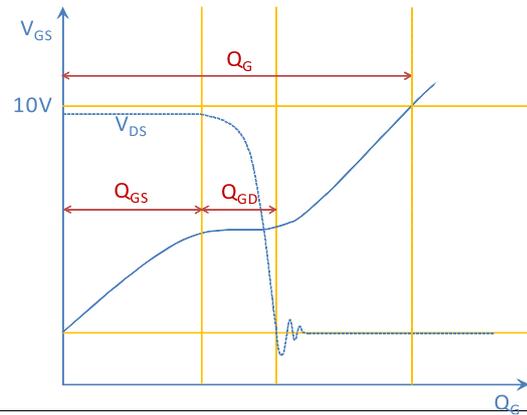
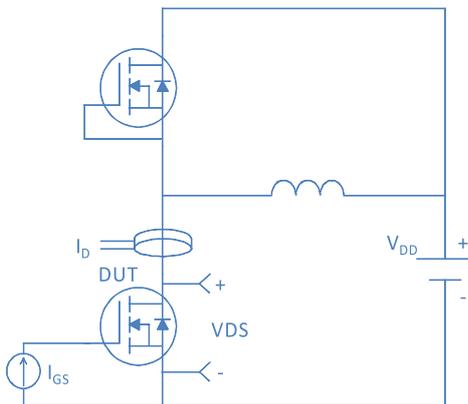
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



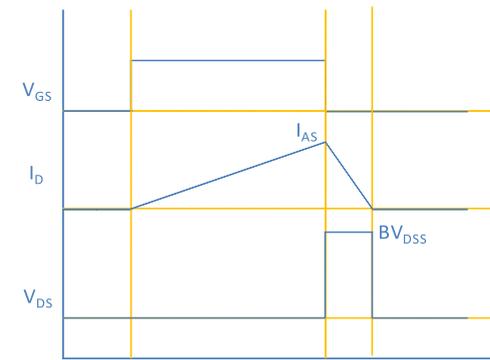
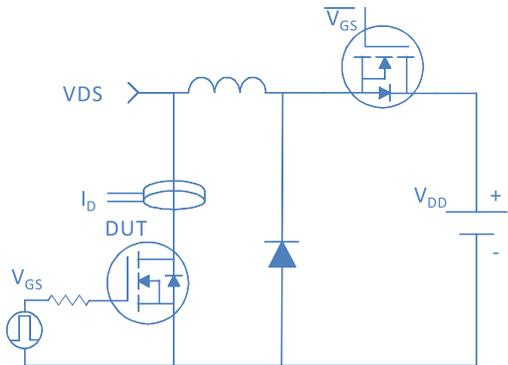
### Inductive switching Test



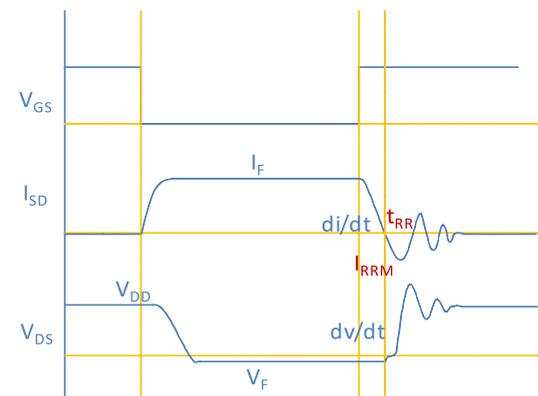
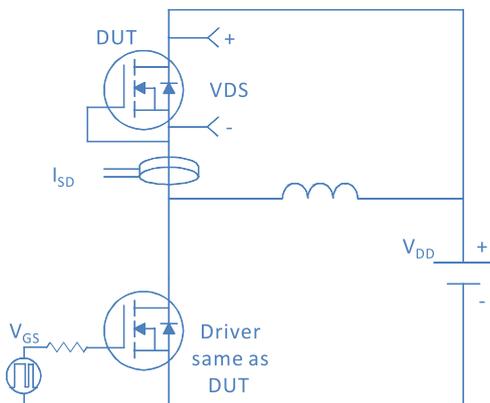
### Gate Charge Test



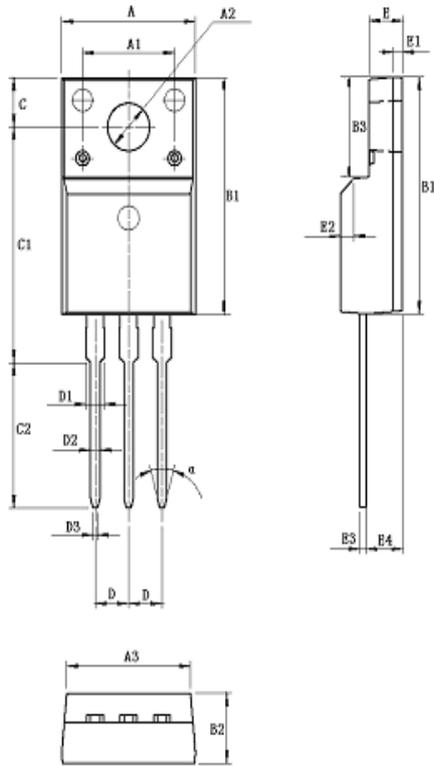
### Uclamped Inductive Switching (UIS) Test



### Diode Recovery Test



TO-220F, 3 leads



Dimensions in mm unless otherwise specified

Symbol	Min	Nom	Max
A	9.96	10.16	10.36
A1		7	
A2	3.08	3.18	3.28
A3	9.26	9.46	9.66
B1	15.67	15.87	16.07
B2	4.50	4.70	4.90
B3	6.48	6.68	6.88
C	3.20	3.30	3.40
C1	15.60	15.80	16.00
C2	9.55	9.75	9.95
D		2.54	
D1			1.47
D2	0.70	0.80	0.90
D3	0.25	0.35	0.45
E	2.34	2.54	2.74
E1		0.70	
E2	1.0x45°		
E3	0.45	0.50	0.60
E4	2.56	2.76	2.96
α (degree)		30°	